

WHAT IS CLAIMED IS:

1. A method for manufacturing a trench isolation structure,
2 comprising:
3 forming a polysilicon hardmask over a substrate;
4 etching a trench in said substrate through said polysilicon
5 hardmask; and
6 filling said trench with an insulative material.

2. The method as recited in Claim 1 further including
2 placing a pad oxide layer between said substrate and said
3 polysilicon hardmask.

3. The method as recited in Claim 2 wherein said pad oxide
2 layer has a thickness ranging from about 10 nm to about 20 nm.

4. The method as recited in Claim 1 further including
2 growing a liner oxide within said trench and over said polysilicon
3 hardmask prior to filling said trench with said insulative
4 material.

5. The method as recited in Claim 4 wherein said grown liner
2 oxide has a thickness ranging from about 10 nm to about 20 nm.

6. The method as recited in Claim 1 wherein filling said
2 trench with an insulative material includes depositing said
3 insulative material within said trench.

7. The method as recited in Claim 1 wherein said polysilicon
2 hardmask has a thickness ranging from about 100 nm to about 200 nm.

8. The method as recited in Claim 1 wherein said trench has
2 a width ranging from about .15 μm to about 20 μm and has a depth
3 ranging from about 0.1 μm to about 0.5 μm .

9. A trench isolation structure formed using said method of
2 Claim 1.

10. A method for manufacturing an integrated circuit,
2 comprising:

3 forming trench isolation structures in a substrate, including;

4 forming a polysilicon hardmask over said substrate; ✓

5 etching a trench in said substrate through said
6 polysilicon hardmask; and

7 filling said trench with an insulative material;

8 forming transistor devices over said substrate; and

9 constructing an interlevel dielectric layer over said
10 transistor devices and having interconnects located therein,
11 wherein said interconnects contact said transistor devices to form
12 an operational integrated circuit.

11. The method as recited in Claim 10 further including
2 placing a pad oxide layer between said substrate and said
3 polysilicon hardmask.

12. The method as recited in Claim 11 wherein said pad oxide
2 layer has a thickness ranging from about 10 nm to about 20 nm.

13. The method as recited in Claim 10 further including
2 growing a liner oxide within said trench and over said polysilicon
3 hardmask prior to filling said trench with said insulative
4 material.

14. The method as recited in Claim 13 wherein said grown
2 liner oxide has a thickness ranging from about 10 nm to about 20
3 nm.

15. The method as recited in Claim 10 wherein filling said
2 trench with an insulative material includes depositing said
3 insulative material within said trench.

16. The method as recited in Claim 10 wherein said
2 polysilicon hardmask has a thickness ranging from about 100 nm to
3 about 200 nm.

17. The method as recited in Claim 10 wherein said trench has
2 a width ranging from about .15 μm to about 20 μm and has a depth
3 ranging from about 0.1 μm to about 0.5 μm .

18. An integrated circuit formed using said method of Claim
2 10.

19. A trench isolation structure, comprising:

2 a substrate having a trench located therein; 3

3 an isolation material located within said trench, wherein said

4 isolation material has no undercut at corners where said isolation

5 material meets said substrate.

20. The trench isolation structure as recited in Claim 19

2 further including a liner oxide located between said trench and

3 said isolation material.